Claims

What is claimed is:

1. A method of processing information in a receiver of a digital communication system, the method comprising the step of:

applying a signal processing operation to a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation corresponding to a rotated version of a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits, and further wherein use of the first modulation constellation allows the signal processing operation to be performed using a reduced number of operations relative to the number of operations required in conjunction with the second modulation constellation.

2. The method of claim 1 wherein use of the first modulation constellation allows the signal processing operation to be performed without multiplication operations.

3. The method of claim 1 wherein the first modulation constellation is generated by applying a 45° rotation to the second modulation constellation.

4. The method of claim 1 wherein the second modulation constellation comprises one of a PSK constellation and a QAM constellation.

5. The method of claim 1 wherein the signal processing operation comprises at least one of a finite impulse response (FIR) filtering operation, a Least-Mean-Squares (LMS) estimation operation, and a Maximum-Likelihood (ML) sequence detection operation using a Viterbi algorithm.

6. The method of claim 1 wherein the signal processing operation utilizes a selector to implement a complex multiplication of a channel estimate coefficient with a symbol from the first modulation constellation.

7. The method of claim 6 wherein the selector receives as inputs real and imaginary parts of an element of the channel estimate coefficient, and generates as outputs real and imaginary parts of a product of the element of the channel estimate coefficient with a corresponding element of a given one of the symbols, without utilizing a multiplication operation.

8. The method of claim 7 wherein the selector comprises first and second switches and first and second add/subtract unit, the first and second switches each selecting one of the real or the imaginary part of the element of the channel estimate coefficient for application to a corresponding one of the add/subtract units, such that the add/subtract units compute elements of real and imaginary parts of an inner vector product.

9. The method of claim 8 wherein an FIR filter operation is implemented using the selector by including feedback from outputs of the add/subtract units to corresponding inputs of the add/subtract units.

10. The method of claim 1 wherein the signal processing operation comprises a multi-stage multiplication operation implemented without multiplication operations, wherein each stage of the multi-stage operation corresponds to a selector, and a left shift element is arranged between an output of a given one of the stages and a corresponding input of a subsequent stage.

11. The method of claim 1 wherein the signal processing operation is implemented utilizing a multi-stage hierarchical adder tree without multiplication operations.

12. An apparatus for use in processing information in a receiver of a digital communication system, the apparatus comprising:

a signal processing circuit for processing a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation corresponding to a rotated version of a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits, and further wherein use of the first modulation constellation

allows the signal processing operation to be performed using a reduced number of operations relative to the number of operations required in conjunction with the second modulation constellation.

13. The apparatus of claim 12 wherein use of the first modulation constellation allows the signal processing operation to be performed without multiplication operations.

14. The apparatus of claim 12 wherein the first modulation constellation is generated by applying a 45° rotation to the second modulation constellation.

15. The apparatus of claim 12 wherein the other modulation constellation comprises one of a PSK constellation and a QAM constellation.

16. The apparatus of claim 12 wherein the signal processing circuit comprises at least one of a finite impulse response (FIR) filter, a Least-Mean-Squares (LMS) estimator, and a Maximum-Likelihood (ML) sequence detector implemented using a Viterbi algorithm.

17. The apparatus of claim 12 wherein the signal processing circuit comprises at least one selector operative to implement a complex multiplication of a channel estimate coefficient with a symbol from the first modulation constellation.

18. The apparatus of claim 17 wherein the selector receives as inputs real and imaginary parts of an element of the channel estimate coefficient, and generates as outputs real and imaginary parts of a product of the element of the channel estimate coefficient with a corresponding element of a given one of the symbols, without utilizing a multiplication operation.

19. The apparatus of claim 18 wherein the selector comprises first and second switches and first and second add/subtract unit, the first and second switches each selecting one of the real or the imaginary part of the element of the channel estimate coefficient for application to a corresponding

one of the add/subtract units, such that the add/subtract units compute elements of real and imaginary parts of an inner vector product.

20. The apparatus of claim 19 wherein the signal processing circuit comprises an FIR filter implemented using the selector configured with feedback from outputs of the add/subtract units to corresponding inputs of the add/subtract units.

21. The apparatus of claim 12 wherein the signal processing circuit comprises a multi-stage circuit implemented without multiplication operations, wherein each stage of the multi-stage circuit corresponds to a selector, and a left shift element is arranged between an output of a given one of the stages and a corresponding input of a subsequent stage.

22. The apparatus of claim 12 wherein the signal processing circuit is implemented utilizing a multi-stage hierarchical adder tree without multiplication operations.

23. An apparatus for use in processing information in a receiver of a digital communication system, the apparatus comprising:

signal processing means for applying a signal processing operation to a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation corresponding to a rotated version of a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits, and further wherein use of the first modulation constellation allows the signal processing operation to be performed using a reduced number of operations relative to the number of operations required in conjunction with the second modulation constellation.

24. A method of processing information in a transmitter of a digital communication system, the method comprising the step of:

generating a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation generated by applying a predetermined

rotation to a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits, and further wherein use of the first modulation constellation allows a signal processing operation in a corresponding receiver of the system to be performed using a reduced number of operations relative to the number of operations required in conjunction with the second modulation constellation.

25. An apparatus for use in processing information in a transmitter of a digital communication system, the apparatus comprising:

means for generating a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation representative of a rotated version of a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits, and further wherein use of the first modulation constellation allows a signal processing operation in a corresponding receiver of the system to be performed using a reduced number of operations relative to the number of operations required in conjunction with the second modulation constellation.